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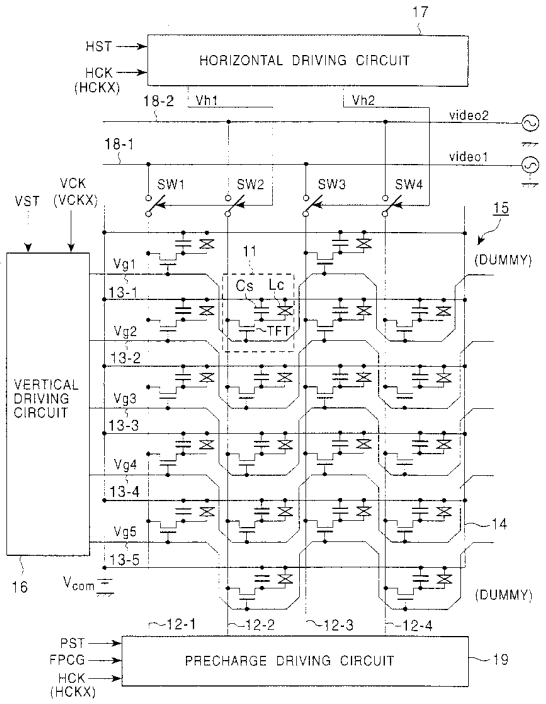
(54) Active matrix display device and method of driving the same

(57) A liquid crystal display driven by a dot-line inversion driving method in combination with a 2-step dot sequential precharge driving method which, if black window or black lines are displayed, is free of horizontal trails on circumscribing portions thereof is provided. Before video signals having opposite polarities are applied to signal lines, first, a full-line precharge pulse is generated in the horizontal blanking periods, and precharge gray signals which have the same polarity as that of the previous pixel potential are written together based on the full-line precharge pulse. Then, precharge black signals having the same polarity as that of one of the video signals, and precharge gray signals having the same polarity of that of the other video signal are written in two steps.

FIG. 1



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Description

[0001] The present invention relates to a display device and a method of driving the same, and more particularly to an active matrix display device which is driven by a dot-line inversion driving method in combination with a dot sequential precharge driving method, and to a method of driving the same.

[0002] One known driving method of a display device having pixels arranged in a matrix, such as an active matrix liquid crystal display (LCD), is a dot sequential driving method in which pixels are sequentially driven for one line (one row) on a pixel-by-pixel basis. The dot sequential driving method includes a 1H inversion driving method and a dot inversion driving method.

[0003] The 1H inversion driving method experiences the following problems. When video signals are written, resistance exists between horizontally adjacent pixels on lines (hereinafter referred to as "Cs lines") which distribute a predetermined dc voltage to pixels as a common voltage V_{com}, and parasitic capacitance exists at intersections of the Cs lines and signal lines. This causes the video signals to jump over onto the Cs lines or gate lines, resulting in oscillations in the potentials of the Cs lines toward the same polarity as those of the video signals. Therefore, significant horizontal crosstalk or defective shading occurs, leading to significant degradation of the picture quality.

[0004] When the pixels maintain pixel information in a period of one field, the potentials of the signal lines oscillate every one horizontal scanning period (1H). In the 1H inversion driving method, the polarities of the video signals written to horizontally adjacent pixels are the same, and the potentials of the signal lines increasingly oscillate. This potential oscillation jumps over to the pixels due to the source-drain coupling of pixel transistors, causing significant vertical crosstalk, resulting in degradation of the picture quality.

[0005] On the other hand, in the dot inversion driving method, video signals having opposite polarities are concurrently written to horizontally adjacent pixels, and the potential oscillations of the Cs lines or the signal lines are cancelled out between the adjacent pixels, thereby solving the degradation problem of the picture quality exhibited by the 1H inversion driving method. However, since the polarities of the video signals written to horizontally adjacent pixels are opposite, the fields of the adjacent pixels produce domains (optically dropped regions) at the edges of apertures in the pixels. As a result, the aperture ratio of the pixels is reduced, thus providing a lower transmittance, leading to a reduction in contrast.

[0006] In order to address such a deficiency, there has been proposed a driving method termed the "dot-line inversion driving method" in which video signals having polarities opposite to each other are concurrently written to two odd-numbered rows of pixels which are spaced apart, e.g., two rows apart vertically, in adjacent pixel columns so that the polarities of horizontally adjacent pixels are the same while the polarities of vertically adjacent pixels are opposite in the array of pixels to which the video signals have been written.

[0007] In the dot-line inversion driving method, video signals having opposite polarities are applied to adjacent signal lines, as in the dot inversion driving method, and the polarities of horizontally adjacent pixels are the same in the array of pixels to which the video signals have been written, as in the 1H inversion driving method. Therefore, degradation of the picture quality due to horizontal crosstalk or shading can be prevented without necessity to reduce the aperture ratio of the pixels.

[0008] However, when video signals written to pixels are inverted every 1H during the dot sequential driving, a significant charging/discharging current when the video signals are written to the signal line extending along each column of pixels would appear as vertical fringes on the display screen. In order to reduce the charging/discharging current during the writing of the video signals as much as possible, a precharge driving method has been adopted in which precharge signals are written in advance before the video signals are written.

[0009] In general, gray levels are most likely to produce visible vertical fringes. Therefore, the precharge signal level is typically set at a gray level which is most likely to produce visible vertical fringes. If the precharge signal level is set at a gray level, however, vertical crosstalk occurs when a window pattern and the like are displayed because the amount of source-drain optical leakage of pixel transistors differs according to location from picture to picture, resulting in degradation of the picture quality.

[0010] In order to prevent such vertical crosstalk, the precharge signal level should be set at the black level, thereby making the source-drain leakage current of the pixel transistors uniform over the entire screen. If the precharge signal level is set at the black level, however, vertical fringes as previously described again appear. In summary, vertical crosstalk and vertical fringes are in a trade-off relation.

[0011] Accordingly, a 2-step dot sequential precharge method has been proposed in which a black-level signal and a gray-level signal are precharged in two steps. Fig. 8 illustrates a circuit structure of a precharge driving circuit 100 in the active matrix liquid crystal display driven by the 2-step dot sequential precharge method.

[0012] In Fig. 8, the precharge driving circuit 100 includes a shift register 101 and a precharge switching circuit 102. When a precharge start pulse PST is input, the shift register 101 shifts or transfers the precharge start pulse PST in turn to shift stages (S/Rs) in synchronization with horizontal clocks HCK and HCKX having opposite phases to each other, and successively outputs it as precharge control pulses PCC1, PCC2, and so on from the shift stages.

[0013] The precharge control pulses PCC1, PCC2, etc. are supplied to the precharge switching circuit 102.

The precharge switching circuit 102 also receives an odd-column precharge black signal PsigBo via a precharge signal line 103o, an even-column precharge black signal PsigBe via a precharge signal line 103e, an odd-column precharge gray signal PsigGo via a precharge signal line 104o, and an even-column precharge gray signal PsigGe via a precharge signal line 104e.

[0014] In the precharge switching circuit 102, a precharge switch 106-1b is connected between a signal line 105-1 of a pixel section and the precharge signal line 103o, a precharge switch 106-1g is connected between the signal line 105-1 and the precharge signal line 104o, a precharge switch 106-2b is connected between a signal line 105-2 of the pixel section and the precharge signal line 103e, and a precharge switch 106-2g is connected between the signal line 105-2 and the precharge signal line 104e. Other precharge switches are further connected in the same way.

[0015] The precharge control pulses PCC1, PCC2, etc. which are output from the shift stages of the shift register 101 are used as drive signals of the precharge switches 106-1b, 106-1g, 106-2b, 106-2g, etc.

[0016] Specifically, the precharge control pulse PCC1 from the first stage is applied to the precharge switch 106-1b as a switch driving pulse PSD1b, the precharge control pulse PCC3 from the third stage is applied to the precharge switch 106-1g as a switch driving pulse PSD1g, the precharge control pulse PCC2 from the second stage is applied to the precharge switch 106-2b as a switch driving pulse PSD2b, and the precharge control pulse PCC4 from the fourth stage is applied to the precharge switch 106-2g as a switch driving pulse PSD2g. Other precharge control pulses are further applied in the same way to the subsequent precharge switches.

[0017] Fig. 9 is a timing chart of the precharge start pulse PST, the horizontal clock HCK, the black-level switch driving pulses PSD1b, PSD2b, PSD3b, PSD4b, and PSD5b, and the gray-level switch driving pulses PSD1g, PSD2g, PSD3g, and PSD4g.

[0018] If black windows or black lines are displayed on an active matrix liquid crystal display driven by the dot-line inversion driving method in combination with the dot sequential precharge driving method, so-called trails in which black lines appear over and along the horizontal scan direction (hereinafter referred to as "horizontal trails") occur on circumscribing portions thereof having a higher contrast in intensity, as shown in Fig. 10. Such horizontal trails can degrade the picture quality. The cause of horizontal trails is described as below.

[0019] In the dot-line inversion driving method, as previously described, the polarity of the input video signal is inverted from positive to negative or vice versa at odd columns and even columns of pixels with reference to the common voltage V_{com} which is commonly supplied to the pixels, and is also inverted every 1H. The resulting polarities of the pixel potentials are shown in Fig. 11, in which pixel potentials which are higher and lower than the common voltage V_{com} are indicated by H and L, respectively.

[0020] If black windows or black lines are displayed, the pixel potentials shown in Fig. 12 are input to the circumscribing portions thereof. In Fig. 12, G represents the gray level and B represents the black level.

[0021] Fig. 13 depicts how the potentials of the signal lines vary when the 2-step dot sequential precharge driving method is considered.

[0022] In this illustration, as an example, the H and L levels of the precharge gray signal are set at 10 V and 5 V, respectively, and the H and L levels of the precharge black signal are set at 13 V and 2 V, respectively. In a pixel signal, typically, the H and L levels. of the gray signal are 9 V and 6 V, respectively, and the H and L levels of the black signal are 13 V and 2 V, respectively.

[0023] Referring to Fig. 13, apparently, the potential of the signal line for an odd column varies in the following order: gray L level of an N-th stage pixel potential, precharge black H level, precharge gray H level, and black H level of an (N+1)-th stage pixel potential. The potential of the signal line for an even column varies in the following order: black H level of an N-th stage pixel potential, precharge black L level, precharge gray L level, and black L level of an (N+1)-th stage pixel potential.

[0024] In this illustration, the potential variations from the N-th stage pixel potential to the precharge black signal level are +7 V for an odd column and -11 V for an even column, and the potential variations cannot be therefore offset. Due to the presence of a potential difference between an odd column and an even column, horizontal trails occur, as described above. Generally, the potential variations of the signal lines are coupled through the parasitic capacitance to gate lines which are connected to rows of gate electrodes of pixel transistors, or to Cs lines which distribute the common voltage V_{com} to the pixels.

[0025] Therefore, if black windows or black lines are displayed using the pixel potentials as shown in Fig. 12, the coupling cannot be offset between an odd column and an even column, causing the oscillations to be carried on the gate lines and the Cs lines. The oscillations are applied to other pixels as well as those in window bands when the video signals are written, thereby causing horizontal trails of the windows.

[0026] Accordingly, it is an object of the present invention to provide a display device driven by a dot-line inversion driving method in combination with a dot sequential precharge driving method which, if black windows or black lines are displayed, is free of horizontal trails on circumscribing portions thereof, and to provide a method of driving the same.

[0027] To this end, according to the present invention, a display device includes a pixel section having pixels arranged in a matrix, a signal line extending along each column of pixels, and a gate line extending across two odd-numbered rows which are spaced apart in adjacent pixel columns. The display device further includes a first driving unit for applying scan pulses to the gate lines

while scanning the pixels of the pixel section in the row direction, a second driving unit for sequentially providing video signals having opposite polarities to adjacent pixels via the signal lines, the pixels being connected to the gate lines to which the scan pulses are applied by the first driving unit, and a third driving unit. The third driving unit first provides constant level precharge signals together in the horizontal blanking periods before the video signals having opposite polarities are applied to the signal lines by the second driving unit, and then sequentially provides a black-level precharge signal and a predetermined color level precharge signal. The black-level precharge signal has the same polarity as that of one of the video signals, and the predetermined color level precharge signal has the same polarity as that of the other video signal.

[0028] When a horizontal scan is performed by the second driving unit, the third driving unit may first provide constant level precharge signals together to the pixels which are selected through a vertical scan performed by the first driving unit in the horizontal blanking periods before video signals having opposite polarities are supplied to the signal lines. Then, the third driving unit may sequentially provide a black-level precharge signal having the same polarity as that of one of the video signals, and a predetermined color level precharge signal having the same polarity as that of the other video signal. Subsequently, the second driving unit may provide the video signals having opposite polarities to the signal lines.

[0029] The invention will be more clearly understood from the following description, given by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram of an active matrix liquid crystal display driven by a dot-line inversion driving method in combination with a 2-step dot sequential precharge driving method according to the present invention;

Fig. 2 is a timing chart of the fundamental operation during the dot-line inversion driving;

Fig. 3 is view showing a relation between the addressing of pixels and the polarities of video signals written to the pixels during the dot-line inversion driving;

Fig. 4 is a block diagram showing a specific structure of a precharge driving circuit according to the present invention;

Fig. 5 is a timing chart which illustrates the circuit operation of the precharge driving circuit according to the present invention;

Fig. 6 is a timing chart of the timing at which a full-line precharge is performed;

Fig. 7 is a potential diagram of the potential variations of signal lines in the precharge operation which involves the full-line precharge;

Fig. 8 is a block diagram of a precharge driving circuit as a conventional example;

Fig. 9 is a timing chart of the circuit operation of the precharge driving circuit;

Fig. 10 is an illustration of the display state when a black window is displayed;

Fig. 11 is view showing the polarities of pixel potentials during the dot-line inversion driving;

Fig. 12 is a view showing, when black windows or black lines are displayed, the pixel potentials of circumscribing portions thereof; and

Fig. 13 is a potential diagram of the potential variations of signal lines during the 2-step dot sequential precharge driving.

[0030] Hereinbelow, preferred embodiments of the present invention are described in detail with reference to the drawings.

[0031] Fig. 1 is a circuit diagram of an active matrix liquid crystal display driven by a dot-line inversion driving method in combination with a 2-step dot sequential precharge driving method according to the present invention. For clarification of illustration, the active matrix liquid crystal display shown in Fig. 1 has a pixel array in a 6-row and 4-column matrix, or a 6×4 matrix, by way of example. It is noted that dummy pixels are arranged every other column in the first and sixth rows such that specific color signals, such as black signals, rather than video signals are written to the pixels.

[0032] In Fig. 1, six rows and four columns of pixels 11 are arranged in a matrix, in which odd columns of pixels are only arranged in the first row as dummy and even columns of pixels are only arranged in the sixth row as dummy. Each of the pixels 11 is formed of a thin film transistor TFT which is a pixel transistor, a liquid crystal cell LC having a pixel electrode connected to the drain electrode of the thin film transistor TFT, and a holding capacitor Cs having one electrode connected to the drain electrode of the thin film transistor TFT.

[0033] Each of signal lines 12-1 to 12-4 extends along the pixel arrangement in a column of pixels 11. On the other hand, each of gate lines 13-1 to 13-5 extends across two odd-numbered rows which are spaced apart, e.g., two lines (rows) apart vertically, in a meandering fashion therebetween, rather than extends along the pixel arrangement in a row of pixels 11.

[0034] Specifically, the gate line 13-1 extends through the first-row and first-column pixel, the second-row and second-column pixel, the first-row and third-column pixel, and the second-row and fourth-column pixel. The gate line 13-2 extends through the second-row and first-column pixel, the third-row and second-column pixel, the second-row and third-column pixel, and the third-row and fourth-column pixel. Likewise, the gate lines 13-3, 13-4, and 13-5 each extend in a meandering fashion between two rows of pixels apart vertically.

[0035] The source electrode (or drain electrode) of the thin film transistor TFT in each of the pixels 11 is connected to the corresponding one of the signal lines 12-1 to 12-4. The counter electrode of the liquid crystal cell

LC and the other electrode of the holding capacitor Cs in each of the pixels 11 are connected to a Cs line 14. The Cs lines 14 are commonly provided in the pixels 11. A predetermined dc voltage is applied to the Cs lines 14 as a common voltage V_{com}.

[0036] A connection relation of the gate lines 13-1 to 13-5 is now described. The gate electrodes of the thin film transistors TFT in odd columns, i.e., the first and third columns, of pixels 11 are connected to the gate lines 13-1 to 13-5 which extend along the corresponding rows (the first to fifth rows). The gate electrodes of the thin film transistors TFT in even columns, i.e., the second and fourth columns, of pixels 11 are connected to the gate lines 13-1 to 13-5 which extend along the rows which are located onerow above with respect to the corresponding rows (the second to sixth rows).

[0037] The pixels 11 are thus arranged into a matrix to form a pixel section 15 in which the signal lines 12-1 to 12-4 extend along columns of pixels 11, and the gate lines 13-1 to 13-5 each extend across two odd-numbered rows which are spaced apart, e.g., two lines (rows) apart vertically, in a meandering fashion therebetween. In the pixel section 15, one end of each of the gate lines 13-1 to 13-5 is connected to an output end of a vertical driving circuit 16 which may be placed to the left with respect to the pixel section 15.

[0038] The vertical driving circuit 16 performs a vertical scan (in the pixel row direction) every one field to sequentially select the pixels 11 which are alternately connected to the gate lines 13-1 to 13-5 across the two rows apart vertically.

[0039] Specifically, when a scan pulse Vg1 is applied from the vertical driving circuit 16 to the gate line 13-1, the first-row and first-column pixel, the second-row and second-column pixel, the first-row and third-column pixel, and the second-row and fourth-column pixel are selected. When a scan pulse Vg2 is applied to the gate line 13-2, the second-row and first-column pixel, the third-row and second-column pixel, the second-row and third-column pixel, and the third-row and fourth-column pixel are selected. When scan pulses Vg3, Vg4, and Vg5 are in turn applied to the gate lines 13-3, 13-4, and 13-5, respectively, the pixels are alternately selected in the horizontal direction (in the pixel column direction) in the same way across the two rows apart vertically. A specific structure of the vertical driving circuit 16 is described later in detail.

[0040] A horizontal driving circuit 17 may be disposed above the pixel section 15. The horizontal driving circuit 17 sequentially samples every 1H, for example, two types of video signals video1 and video2 to write the result to the pixels 11 which are selected by the vertical driving circuit 16. The two types of video signals video1 and video2 may be video signals having polarities which are inverted every 1H and which are opposite with respect to a reference voltage (common voltage V_{com}). As defined herein, the video signal having a higher potential than the common voltage V_{com} is positive (H) and the video signal having a lower potential is negative (L).

[0041] Sampling switches SW1 and SW3 are connected between a video line 18-1 through which the video signal video1 is input and, for example, the odd-column signal lines 12-1 and 12-3 of the pixel section 15, respectively. Sampling switches SW2 and SW4 are connected between a video line 18-2 through which the video signal video2 is input and the even-column signal lines 12-2 and 12-4 of the pixel section 15, respectively.

[0042] The sampling switches SW1 and SW2 are paired, and the sampling switches SW3 and SW4 are paired. In response to sampling pulses Vh1 and Vh2 which are output in turn from the horizontal driving circuit 17, the pairs of sampling switches SW1 and SW2, and SW3 and SW4 are sequentially turned on, so that the two types of video signals video1 and video2 having polarities opposite to each other may be written via the signal lines 12-1 to 12-4 on a two-column (two-pixel) basis.

[0043] A precharge driving circuit 19 may be disposed below the pixel section 15. The precharge driving circuit 19 serves to write a black-level precharge signal and a predetermined color level precharge signal, such as a gray-level precharge signal, in a 2-step dot sequential manner in advance before the video signals video1 and video2 are written, in order to reduce a charging/discharging current due to the writing of the video signals video1 and video2 as much as possible. A specific structure and operation of the precharge driving circuit 19 are described later in detail.

[0044] Now, the fundamental operation of the active matrix liquid crystal display driven by the dot-line inversion driving method in combination with the 2-step dot sequential precharge driving method according to the present invention is described with reference to a timing chart shown in Fig. 2. The addressing of the pixels 11 in the 6×4 pixel array is shown in Fig. 3, in which symbol "d" represents a dummy pixel.

[0045] In the first line, when the scan pulse Vg1 is output from the vertical driving circuit 16, the scan pulse Vg1 is applied to the gate electrodes of the thin film transistors TFT in the pixels d-1, 1-2, d-3, and 1-4 via the gate line 13-1, to turn on the pixels d-1, 1-2, d-3, and 1-4.

[0046] At this time, the video signals video1 and video2 having polarities opposite to each other are input via the video lines 18-1 and 18-2, and the sampling pulses Vh1 and Vh2 are output in turn from the horizontal driving circuit 17. Hence, the pairs of sampling switches SW1 and SW2, and SW3 and SW4 are sequentially turned on.

[0047] The video signals video1 and video2 having polarities opposite to each other are first applied to the signal lines 12-1 and 12-2 through the sampling switches SW1 and SW2, respectively. Therefore, the video signal video1 having the negative polarity, as is indicated by L in Fig. 3, is written to the pixel d-1, and the video signal video2 having the positive polarity, as is indicated by H in Fig. 3, is written to the pixel 1-2. It-is noted that the video signal video1 to be input is implemented as a

black signal, and the black signal is written to the dummy pixel d-1.

[0048] Then, the video signals video1 and video2 are applied to the signal lines 12-3 and 12-4 through the sampling switches SW3 and SW4, respectively. Therefore, the video signal videol having the negative polarity is written to the pixel d-3, and the video signal video2 having the positive polarity is written to the pixel 1-4. It is also noted that the video signal video1 to be input is implemented as a black signal, and the black signal is written to the dummy pixel d-3.

[0049] In the second line, when the scan pulse Vg2 is output from the vertical driving circuit 16, the scan pulse Vg2 is applied to the gate electrodes of the thin film transistors TFT in the pixels 1-1, 2-2, 1-3, and 2-4 via the gate line 13-2 to turn on the pixels 1-1, 2-2, 1-3, and 2-4. In the second line, the polarities of the video signals video1 and video2 are inverted with respect to the reference potential.

[0050] That is, the video signal video1 becomes positive and the video signal video2 becomes negative in the second line, although the video signal video1 is negative and the video signal video2 is positive in the first line. As the sampling pulses Vh1 and Vh2 are again output in turn from the horizontal driving circuit 17, the pairs of sampling switches SW1 and SW2, and SW3 and SW4 are sequentially turned on.

[0051] The video signals video1 and video2 having polarities opposite to each other are first applied to the signal lines 12-1 and 12-2 through the sampling switches SW1 and SW2, respectively. Therefore, the video signal video1 having the positive polarity is written to the pixel 1-1, and the video signal video2 having the negative polarity is written to the pixel 2-2. Subsequently, the video signals video1 and video2 are applied to the signal lines 12-3 and 12-4 through the sampling switches SW3 and SW4, respectively. Therefore, the video signal video1 having the positive polarity is written to the pixel 1-3, and the video signal video2 having the negative polarity is written to the pixel 2-4.

[0052] In the subsequent procedure, the polarities of the video signals video1 and video2 having polarities opposite to each other are inverted every 1H with respect to the reference potential and input, and the above-described operation is repeatedly performed until the scan in the pixel row direction (vertical scan) performed by the vertical driving circuit 16 and the scan in the pixel column direction (horizontal scan) performed by the horizontal driving circuit 17 are completed. It is noted that when the gate line 13-5 is scanned, the video signals video2 to be input are implemented as black signals, and the black signals are written-to the dummy pixels d-2 and d-4.

[0053] Accordingly, in the dot-line inversion driving method, for example, when two types of video signals video1 and video2 having polarities opposite to each other with respect to a reference potential are input, the video signals video1 and video2 having opposite polarities are concurrently written to two odd-numbered rows (two rows apart vertically in this example) of pixels which are spaced apart in adjacent pixel columns so that the polarities of vertically adjacent pixels are the same while the polarities of the vertically adjacent pixels are opposite in the array of pixels to which the-video signals have been written, as shown in Fig. 3. The dot-line inversion driving method would achieve the following advantages.

[0054] As is apparent from the timing chart shown in Fig. 2, when the sampling pulses Vh1 and Vh2 are successively output to sequentially turn on the pairs of sampling switches SW1 and SW2, and SW3 and SW4, the video signals video1 and video2 having polarities opposite to each other with respect to a reference potential are applied to the signal lines 12-1 and 12-3 and the signal lines 12-2 and 12-4, respectively. Therefore, degradation in the picture quality including horizontal crosstalk, defective shading, and vertical crosstalk can be prevented.

[0055] Specifically, the video signals video1 and video2 having polarities opposite to each other are applied to adjacent signal lines 12-1 to 12-4, thereby making it possible to prevent the deficiency which results from the presence of resistance across the pixels 11 on the Cs lines 14 such that the video signals video1 and video2 jump over onto the Cs lines 14 through the parasitic capacitance at intersections of the signal lines 12-1 to 12-4 and the Cs lines 14, or through the holding capacitor Cs of the pixels 11. There occurs no oscillation in the potential of the Cs lines 14. Therefore, the horizontal crosstalk or defective shading problem can be overcome.

[0056] Furthermore, the video signals video1 and video2 having polarities opposite to each other are applied to adjacent signal lines 12-1 to 12-4, thereby making it possible to prevent the deficiency which results from the presence of parasitic capacitance between the source-drain electrodes of the thin film transistors TFT and the signal lines 12-1 to 12-4 such that the potentials of the signal lines 12-1 to 12-4 which oscillate every 1H jump over to the pixels 11 due to the source-drain coupling of the thin film transistors TFT. This prevents vertical crosstalk. Therefore, the video signals video1 and video2 can be written at the -sufficient level, thereby improving the contrast.

[0057] Furthermore, in the illustrated embodiment, the video signals video1 and video2 having polarities opposite to each other are written to the pixels every other column (every other pixel) across different two lines (two lines apart vertically in this example), rather than the pixels on one line in the horizontal direction as in the dot inversion driving method. Hence, the polarities of horizontally adjacent pixels in the array of pixels to which the video signals have been written are the same, as shown in Fig. 3, thereby preventing the domain problem exhibited by the dot inversion driving method. Therefore, no need exists to reduce the aperture rate of the pixels, and the contrast is no longer reduced.

[0058] While the two types of video signals video1 and video2 are input in the illustrated embodiment, the number of video signal inputs is not limited to two, but may be 2m, where m is an integer. Although the video signals video1 and video2 having opposite polarities are concurrently written to two rows of pixels apart vertically in the illustrated embodiment, they are not necessarily written to two rows of pixels apart vertically. What is merely required is that the video signals are concurrently written to pixels on different horizontal lines so that the polarities of the horizontally adjacent pixels may be the same and the polarities of the vertically adjacent pixels may be opposite in the array of pixels to which the video signals have been written.

[0059] While an implementation of a liquid crystal display incorporating an analog interface driving circuit which receives and samples an analog video signal to drive pixels in a dot-sequential manner has been described in the illustrated embodiment, the present invention is not limited on this type of device. The present invention may also be applied to a liquid crystal display incorporating a digital interface driving circuit which receives and latches a digital video signal, converts the latched digital video signal into an analog video signal, and samples the resulting signal to drive pixels in a dot-sequential manner.

[0060] In the active matrix liquid crystal display driven by the dot-line inversion driving method in combination with the 2-step dot sequential precharge driving method as described above, the present invention is directed to a specific structure of the precharge driving circuit 19 and a driving method thereof.

[0061] Fig. 4 is a block diagram showing a specific structure of the precharge driving circuit 19. In. Fig. 4, the precharge driving circuit 19 includes a shift register 21, a logic gate circuit 22, and a precharge switching circuit 23.

[0062] The shift register 21 receives a precharge start pulse PST which commands to start the precharge, and horizontal clocks HCK and HCKX having phases opposite to each other according to which the horizontal scan is performed by the horizontal driving circuit 17. When the precharge start pulse PST is input, the shift register 21 shifts the precharge start pulse PST in turn to shift stages (S/Rs) in synchronization with the horizontal clocks HCK and HCKX, and successively outputs it as precharge control pulses PCC1, PCC2, and so on from the shift stages.

[0063] The precharge control pulses PCC1, PCC2, etc. are supplied to the logic gate circuit 22. The logic gate circuit 22 also receives a full-line precharge pulse FPCG which has been inverted by an inverter 24, as is described later. The logic gate circuit 22 includes NAND gates 221-1, 221-2, and so on which correspond to the signal lines 12-1, 12-2, and so on of the pixel section 15, and inverters 222-1, 222-2, 222-3, and so on.

[0064] In the logic gate circuit 22, the full-line precharge pulse FPCG which has been inverted by the inverter 24 is applied to first inputs, and the precharge control pulses PCC3, PCC4, etc. successively output from the third and subsequent shift stages (S/Rs) are applied to second inputs of the NAND gates 221-1, 221-2, etc.

[0065] Typically, the full-line precharge pulse PFCG is in L level, so that the first inputs of the NAND gates 221-1, 221-2, etc. are in H level, and the second inputs of the NAND gates 221-1, 221-2, etc. are in H level. When the precharge control pulses PCC3, PCC4, etc. are successively output from the third and subsequent shift stages of the shift register 21 to apply L-level pulses to the second inputs of the NAND gates 221-1, 221-2, etc., H-level pulses are sequentially output from the NAND gates 221-1, 221-2, etc.

[0066] The precharge switching circuit 23 receives an odd-column precharge black signal PsigBo via a precharge signal line 25o, an even-column precharge black signal PsigBe via a precharge signal line 25e, an odd-column precharge gray signal PsigGo via a precharge signal line 26o, and an even-column precharge gray signal PsigGe via a precharge signal line 26e.

[0067] In the precharge switching circuit 23, a precharge switch 27-1b is connected between the signal line 12-1 of the pixel section 15 and the precharge signal line 25o, a precharge switch 27-1g is connected between the signal line 12-1 and the precharge signal line 26o, a precharge switch 27-2b is connected between the signal line 12-2 and the precharge signal line 25e, and a precharge switch 27-2g is connected between the signal line 12-2 and the precharge signal line 26e. Other precharge switches are further connected in the same way.

[0068] The precharge control pulses PCC1, PCC2, PCC3, etc. which are output from the shift stages of the shift register 21, and the output pulses of the NAND gates 221-1, 221-2, 221-3, etc. in the logic gate circuit 22 are used as drive signals of the precharge switches 27-1b, 27-1g, 27-2b, 27-2g, etc.

[0069] Specifically, the precharge control pulse PCC1 from the first stage is applied to the precharge switch 27-1b as a switch driving pulse PSD1b, the output pulse of the NAND gate 221-1 is applied to the precharge switch 27-1g as a switch driving pulse PSD1g, the precharge control pulse PCC2 from the second stage is applied to the precharge switch 27-2b as a switch driving pulse PSD2b, and the output pulse of the NAND gate 221-2 is applied to the precharge switch 27-2g as a switch driving pulse PSD2g. Other precharge control pulses or output pulses are further applied in the same way to the subsequent precharge switches.

[0070] Fig. 5 is a timing chart of an enable pulse ENB, the full-line precharge pulse FPCG, the precharge start pulse PST, the horizontal clock HCK, the black-level switch driving pulses PSD1b, PSD2b, PSD3b, PSD4b, and PSD5b, and the gray-level switch driving pulses PSD1g, PSD2g, PSD3g, and PSD4g.

[0071] The enable pulse ENB is generated in a period

of 1H. While the vertical scan is performed by the vertical driving circuit 16, the write operation of the video signals video1 and video2 to one row of pixels is allowed on a row-by-row basis when the enable pulse ENB is in H level. In the L-level duration during which the write operation on a row proceeds to the write operation on another row, the pixel transistors (thin film transistors TFT) are turned off, and the write operation of the video signals videol and video2 to the pixels 11 is prohibited.

[0072] As can be seen from a timing chart shown in Fig. 6, the L-level duration of the enable pulse ENB continues in a part of a horizontal blanking period of approximately 2.9 μsec. In the timing chart shown in Fig. 6, HST represents a horizontal start pulse which commands to start the horizontal scan, VCK represents a vertical clock according to which the vertical scan is performed, and FRP represents a timing pulse which causes the polarities of the video signals video1 and video2 to be inverted.

[0073] In the timing relation shown in Fig. 6, the full-line precharge pulse FPCG is turned H level in the horizontal blanking period, preferably in a portion of the L-level duration of the enable pulse ENB, for example, in synchronization with the vertical clock VCK. The various timing signals including the full-line precharge pulse FPCG are generated by a timing generating circuit (not shown).

[0074] While the horizontal scan is performed by the horizontal driving circuit 17, the precharge driving circuit 19 according to the present invention performs a full-line precharge, as is described later, before the video signals video1 and video2 having polarities opposite to each other are written to the signal lines 12-1, 12-2, etc. The precharge driving circuit 19 also performs a 2-step precharge in which the precharge black signal PsigBo and the precharge gray signal PsigGo which are input with the same polarity as that of the video signal video1, and the precharge black signal PsigBe and the precharge gray signal PsigGe which are input with the same polarity as that of the video signal video2 are written to the signal lines 12-1, 12-2, etc.

[0075] The precharge operation of the precharge driving circuit 19 is described with reference to the timing chart shown in Fig. 5.

[0076] First, the full-line precharge operation is described. As the full-line precharge pulse FPCG is input in the horizontal blanking period, e.g., in the L-level duration of the enable signal ENB, the full-line precharge pulse FPCG passes through the NAND gates 221-1, 221-2, etc. in the logic gate circuit 22, and is concurrently applied to the precharge switches 27-1g, 27-2g, etc. as the gray-level switch driving pulses PSD1g, PSD2g, etc. This allows the precharge switch 27-1g, 27-2g, etc. to be turned on at one time, thereby writing the precharge gray signals having the same polarity as that of the previous-stage pixel potential to all of the signal lines 12-1, 12-2, etc.

[0077] In order to prevent the precharge gray signals PsigGo and PsigGe from being written to the pixels 11, as shown in the timing chart in Fig. 6, the full-line precharge pulse FPCG should be caused to initiate after the timing of the trailing edge of the enable signal ENB and to terminate before the timing of the leading edge of the timing pulse FRP in order to write the precharge gray signals having the same polarity as that of the previous-stage pixel potential.

[0078] Fig. 7 shows how the potentials of signal lines vary during the precharge operation which involves the full-line precharge.

[0079] In this illustration, as an example, the H and L levels of the dot-sequential precharge gray signal are set at 10 V and 5 V, respectively, the H and L levels of the dot-sequential precharge black signal are set at 13 V and 2 V, respectively, and the H and L levels of the full-line precharge gray signal are set at 10 V and 5 V, respectively. In a pixel signal, typically, the H and L levels of the gray signal are 9 V and 6 V, respectively, and the H and L levels of the black signal are 13 V and 2 V, respectively.

[0080] As is apparent from the potential variations of the signal lines shown in Fig. 7, in the horizontal blanking periods during which no video signal is written to the pixels 11, the full-line precharge is performed to individually write a precharge gray signal having constant levels (the H level is 10 V and the L level is 5 V in this example) to the signal lines 12-1, 12-2, etc., thereby making the potential amplitude of the signal lines 12-1, 12-2, etc. equal between odd columns and even columns with respect to the common potential V_{com}.

[0081] Accordingly, the potential variations of the signal lines 12-1, 12-2, etc. are +8 V for an odd column and -8 V for an even column when the dot-sequential precharge black signals are written later, of which the absolute values are equal. Therefore, the coupling from the signal lines 12-1, 12-2, etc. to the Cs lines 14 or the gate lines 13-1, 13-2, etc. can be completely cancelled out. As a result, no oscillation is applied to the Cs lines 14 or the gate lines 13-1, 13-2, etc., and no horizontal trail resulting from such an oscillation occurs.

[0082] Meanwhile, the potential variations from the N-th stage pixel potential to the full-line precharge signal level are -1 V for an odd column and -3 V for an even column, of which the absolute values are different. Therefore, the coupling from the signal lines 12-1, 12-2, etc. to the Cs lines 14 or the gate lines 13-1, 13-2, etc. cannot be cancelled out, and oscillations are carried on the Cs lines 14 and the gate lines 13-1, 13-2, etc. However, the full-line precharge is performed in the horizontal blanking periods during which the pixel transistors (thin film transistors TFT) are turned off, and such oscillations are not applied in the horizontal blanking periods. Consequently, there occurs no horizontal trail resulting from the oscillations applied to the Cs lines 14 or the gate lines 13-1, 13-2, etc.

[0083] In the illustrated embodiment, the precharge signal for the full-line precharge is implemented as a

precharge gray signal (5 V) having the same polarity as that of the previous-stage pixel potential. However, the signal level is arbitrary, and the signal may not necessarily have the same polarity as that of the previous-stage pixel potential. Since the full-line precharge is performed in an extremely short period of the horizontal blanking periods, preferably, the signal has the same polarity as that of the previous-stage pixel potential in order to ensure the write of the dot-sequential precharge black signal immediately after the full-line precharge.

[0084] Next, the 2-step dot sequential precharge operation is described. When the precharge start pulse PST is applied to the shift register 21, the precharge control pulses PCC1, PCC2, PCC3, etc. are sequentially output from the shift stages of the shift register 21 in synchronization with the horizontal clocks HCK and HCKX.

[0085] The precharge control pulses PCC1, PCC2, etc. are sequentially applied to the precharge switches 27-1b, 27-2b, etc. as the black-level switch driving pulses PSD1b, PSD2b, etc. The output pulses of the NAND gates 221-1, 221-2, etc. are sequentially applied to the precharge switches 27-1g, 27-2g, etc. as the gray-level switch driving pulses PSD1g, PSD2g, etc.

[0086] With the series of operations, before the video signals video1 and video2 having polarities opposite to each other are written to the pixels, the precharge black signal PsigBo and the precharge gray signal PsigGo which are input with the same polarity as that of the video signal video1, and the precharge black signal PsigBe and the precharge gray signal PsigGe which are input with the same polarity as that of the video signal video2 can be written in two steps to each row of pixels which is selected through the vertical scan performed by the vertical driving circuit 16.

[0087] Although an implementation of a liquid crystal display using liquid crystal cells as display elements of pixels has been described by way of example in the illustrated embodiment, the present invention is not limited to the implementation of the liquid crystal display. The present invention may be generally applied to display devices driven by the dot-line inversion driving method in combination with the dot sequential precharge dive method.

[0088] According to the present invention, therefore, in a display device driven by the dot-line inversion driving method in combination with the dot sequential precharge driving method, during the horizontal scan, before video signals having polarities opposite to each other are supplied to signal lines, constant level precharge signals are all together written in the horizontal blanking periods, followed by a 2-step precharge. This can cancel out the coupling from the signal lines to Cs lines or gate lines in the write operation of precharge black signals. Therefore, if black windows or black lines are displayed, there occurs no horizontal trail on circumscribing portions thereof.

Claims

1. A display device comprising:

   a pixel section having pixels arranged in a matrix, a signal line extending along each column of pixels, and a gate line extending across two odd-numbered rows which are spaced apart in adjacent pixel columns;
   first driving means for applying scan pulses to the gate lines while scanning the pixels of said pixel section in the row direction;
   second driving means for sequentially providing video signals having opposite polarities to adjacent pixels via the signal lines, the pixels being connected to the gate lines to which the scan pulses are applied by said first driving means; and
   third driving means for providing constant level precharge signals together in the horizontal blanking periods before the video signals having opposite polarities are applied to the signal lines by said second driving means, and then sequentially providing a black-level precharge signal and a predetermined color level precharge signal, the black-level precharge signal having the same polarity as that of one of the video signals and the predetermined color level precharge signal having the same polarity as that of the other video signal.

2. A display device according to Claim 1, wherein said third driving means provides the constant level precharge signals together when pixel transistors in said pixel section are turned off.

3. A display device according to Claim 1 or 2, wherein the constant level precharge signals have the same polarity as that of the previous signal line potential, and each of the constant level precharge signals is the predetermined color level precharge signal.

4. A display device according to Claim 3, wherein the predetermined color level is a gray level.

5. A display device according to Claim 1, 2, 3 or 4 wherein the pixels include display elements, the display elements comprising liquid crystal cells.

6. A method of driving a display device, for writing video signals having polarities opposite to each other to two odd-numbered rows of pixels which are spaced apart in adjacent pixel columns so that the polarities of the horizontally adjacent pixels are the same while the polarities of the vertically adjacent pixels are opposite in the array of pixels to which the video signals have been written, said method comprising the steps of:

providing constant level precharge signals together in the horizontal blanking periods during the horizontal scan before the video signals having opposite polarities are applied to signal lines; and
then sequentially providing a black-level precharge signal and a predetermined color level precharge signal, the black-level precharge signal having the same polarity as that of one of the video signals and the predetermined color level precharge signal having the same polarity as that of the other video signal.

7. A method according to Claim 6, wherein pixel transistors are turned off when the constant level precharge signals are provided together.

8. A method according to Claim 6 or 7, wherein the constant level precharge signals have the same polarity as that of the previous signal line potential, and each of the constant level precharge signals is the predetermined color level precharge signal.

9. A method according to Claim 8, wherein the predetermined color level is a gray level.

10. A method according to Claim 6, 7, 8 or 9 wherein the pixels include display elements, the display elements comprising liquid crystal cells.

FIG. 1

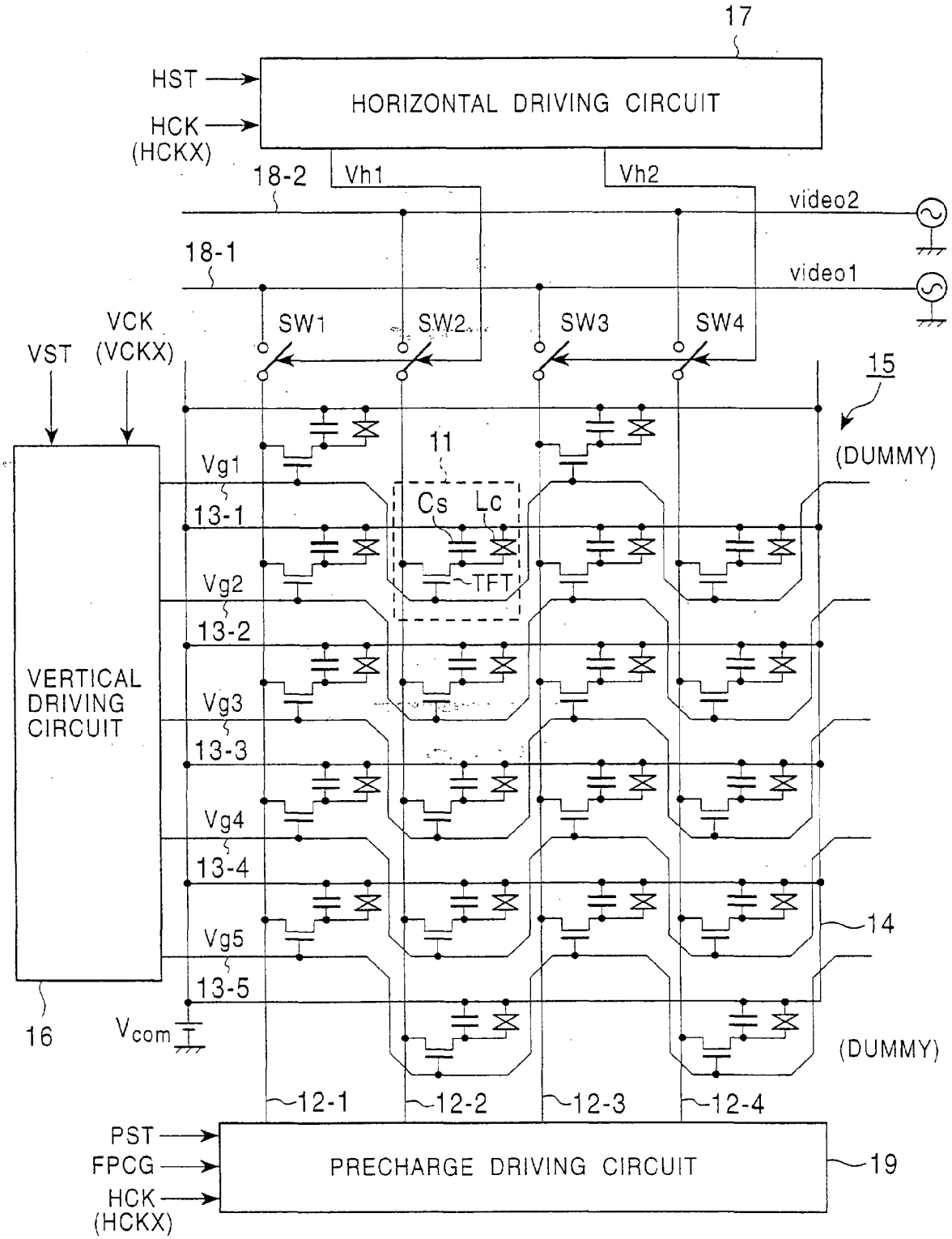

17
HST
HCK
(HCKX)
HORIZONTAL DRIVING CIRCUIT
18-2
Vh1
Vh2
video2
18-1
video1
VST
VCK
(VCKX)
SW1
SW2
SW3
SW4
15
(DUMMY)
11
Vg1
13-1
Cs
Lc
TFT
Vg2
13-2
Vg3
13-3
Vg4
13-4
Vg5
13-5
VERTICAL
DRIVING
CIRCUIT
14
16
Vcom
(DUMMY)
12-1
12-2
12-3
12-4
PST
FPCG
HCK
(HCKX)
PRECHARGE DRIVING CIRCUIT
19

FIG. 2

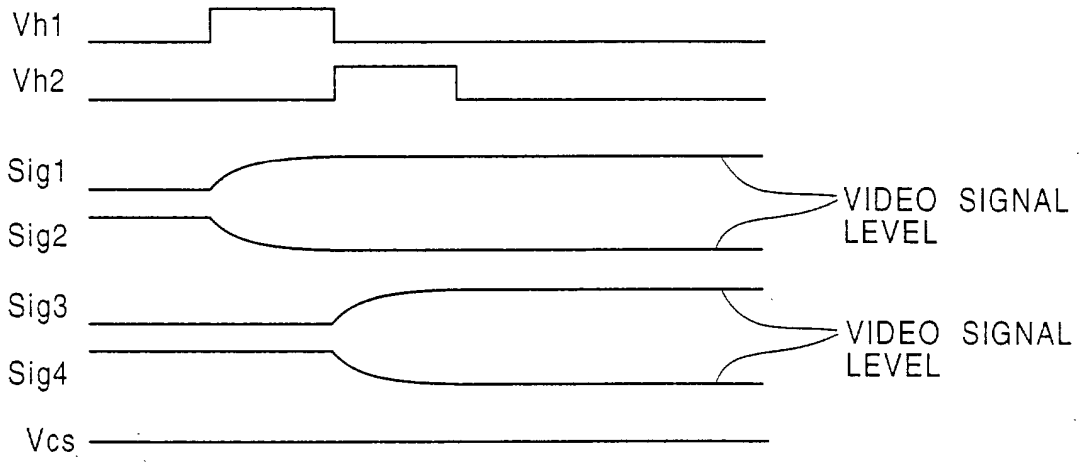


FIG. 3

(d-1) L		(d-3) L		(DUMMY)
(1-1) H	(1-2) H	(1-3) H	(1-4) H	FIRST ROW
(2-1) L	(2-2) L	(2-3) L	(2-4) L	SECOND ROW
(3-1) H	(3-2) H	(3-3) H	(3-4) H	THIRD ROW
(4-1) L	(4-2) L	(4-3) L	(4-4) L	FOURTH ROW
	(d-2) H		(d-4) H	(DUMMY)

FIG. 4

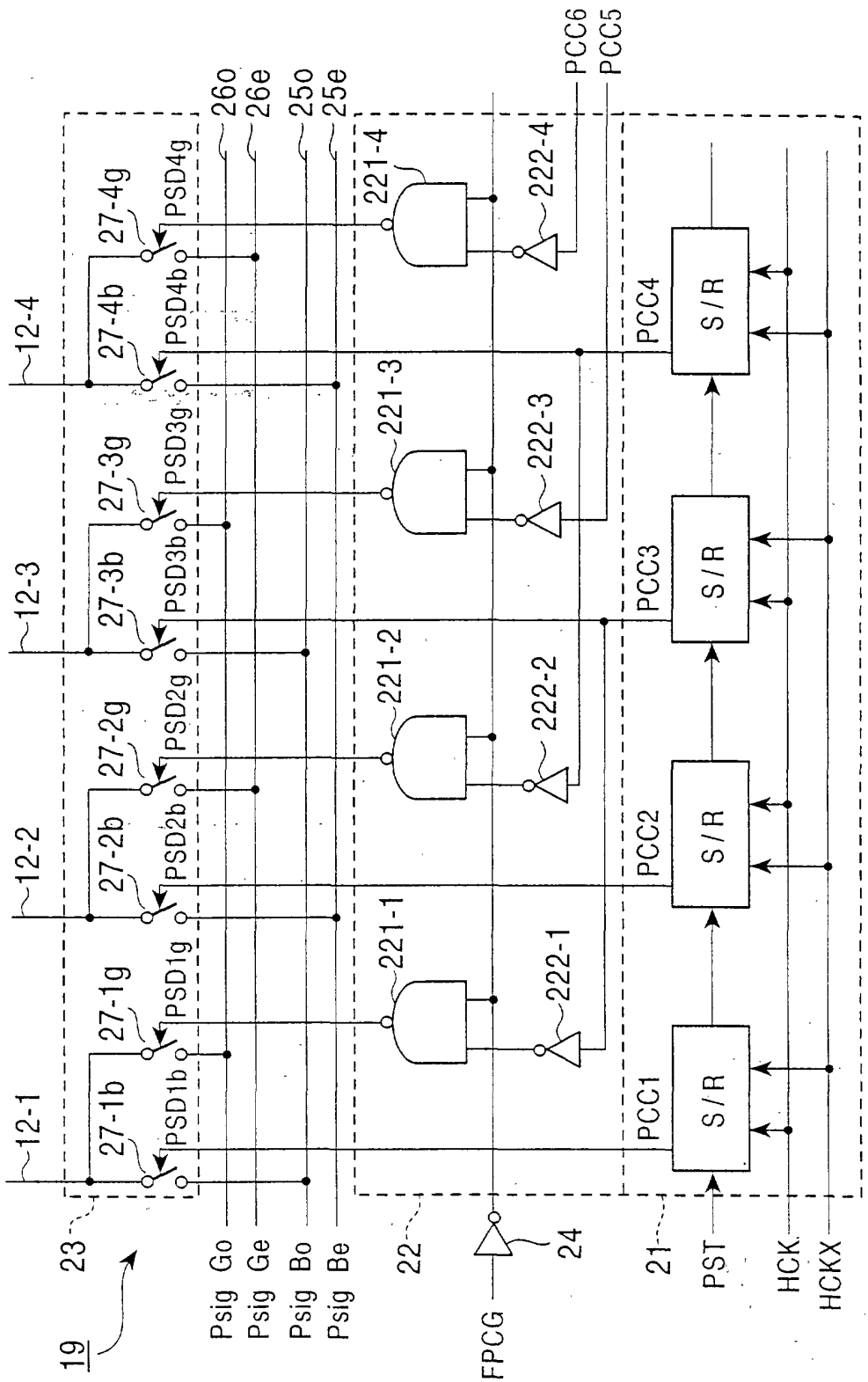

19
23
12-1
12-2
12-3
12-4
27-1b
27-1g
27-2b
27-2g
27-3b
27-3g
27-4b
27-4g
PSD1b
PSD1g
PSD2b
PSD2g
PSD3b
PSD3g
PSD4b
PSD4g
260
26e
250
25e
Psig Go
Psig Ge
Psig Bo
Psig Be
221-1
221-2
221-3
221-4
222-1
222-2
222-3
222-4
22
FPCG
24
PCC6
PCC5
PCC4
PCC3
PCC2
PCC1
S/R
21
PST
HCK
HCKX

FIG. 5

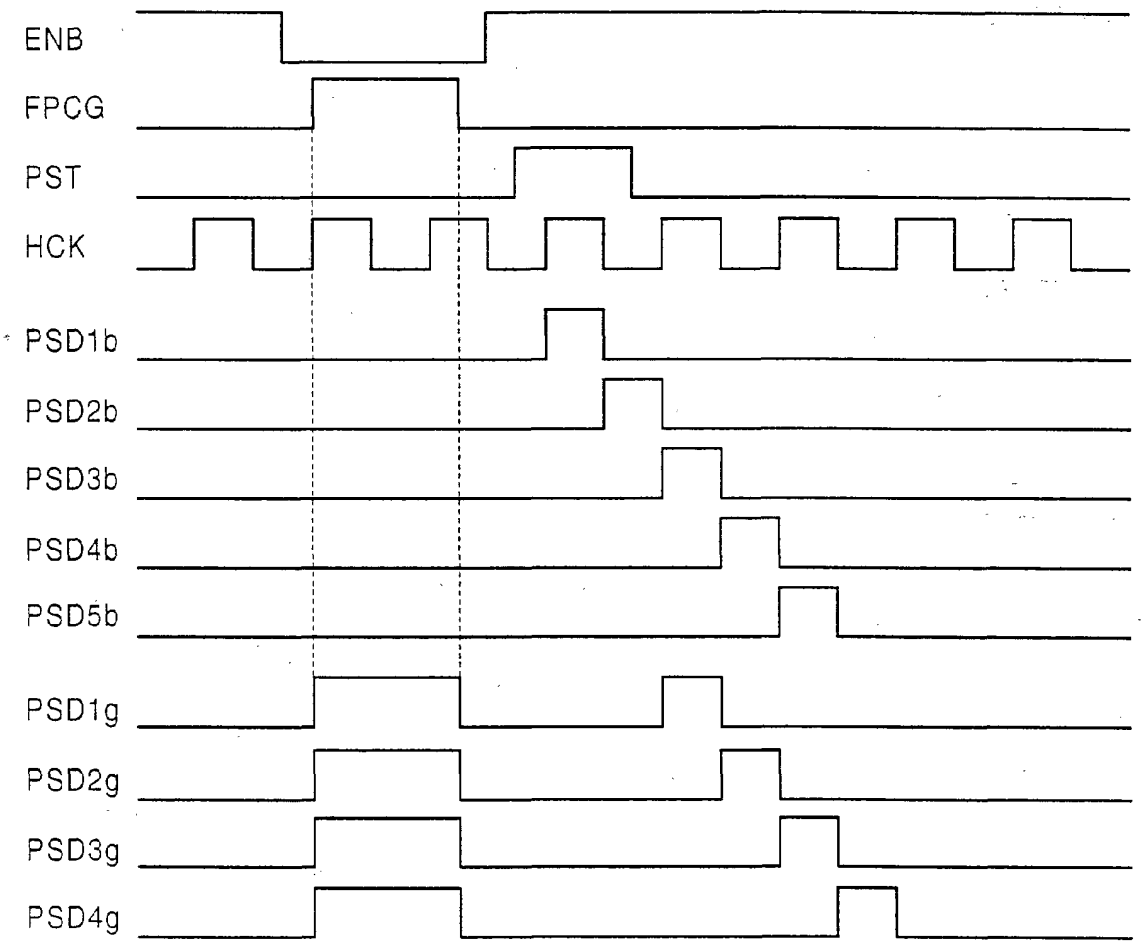

ENB
FPCG
PST
HCK
PSD1b
PSD2b
PSD3b
PSD4b
PSD5b
PSD1g
PSD2g
PSD3g
PSD4g

FIG. 6

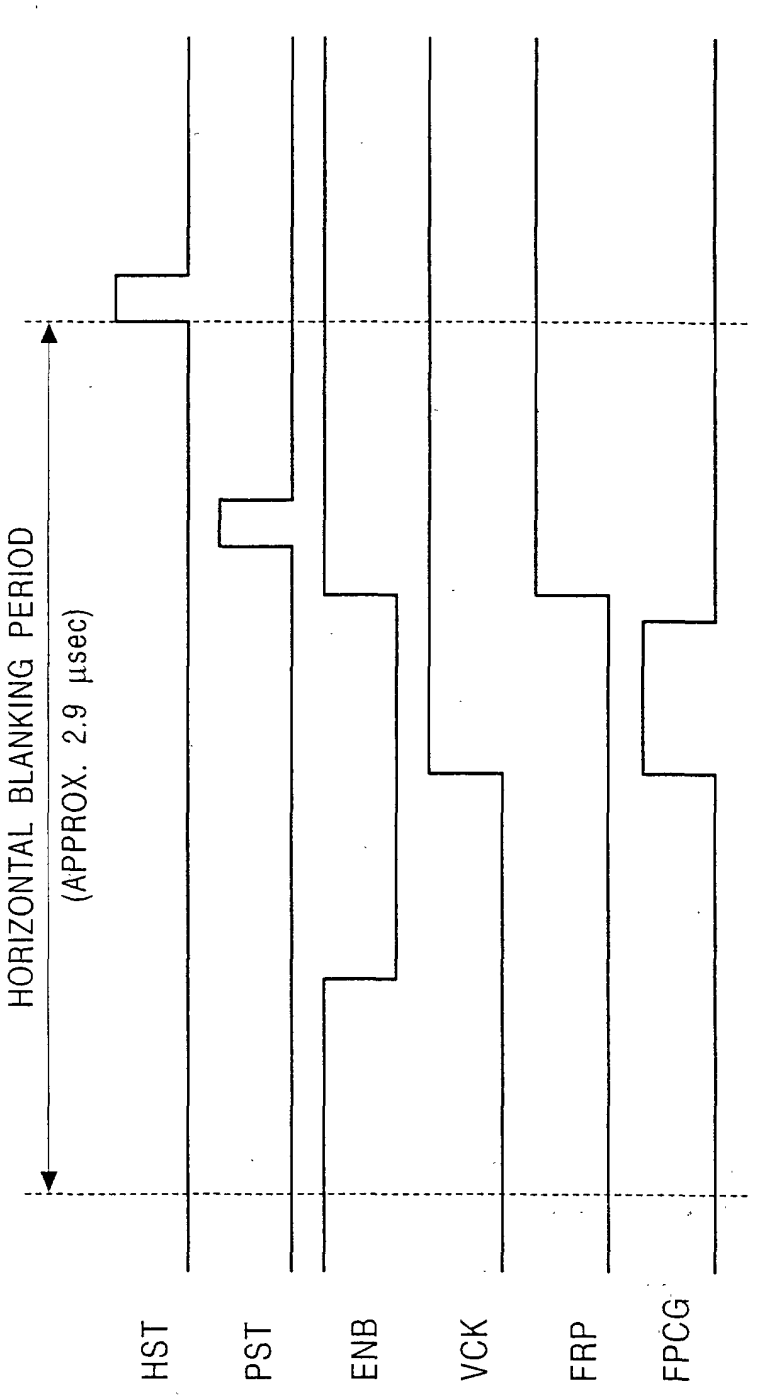

HORIZONTAL BLANKING PERIOD
(APPROX. 2.9 μsec)
HST
PST
ENB
VCK
FRP
FPCG

FIG. 7

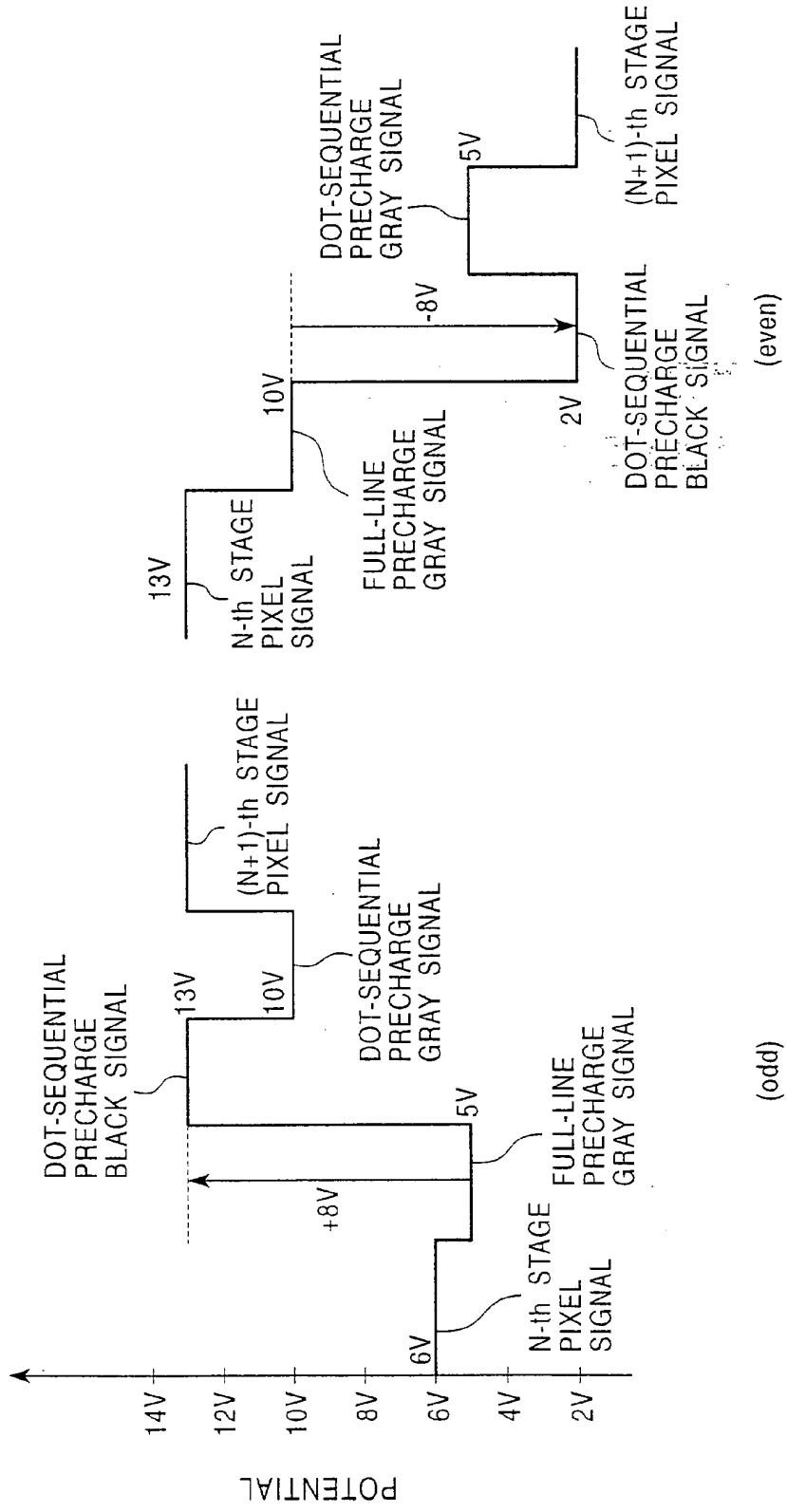

POTENTIAL
14V
12V
10V
8V
6V
4V
2V
DOT-SEQUENTIAL PRECHARGE BLACK SIGNAL
13V
10V
(N+1)-th STAGE PIXEL SIGNAL
DOT-SEQUENTIAL PRECHARGE GRAY SIGNAL
+8V
5V
FULL-LINE PRECHARGE GRAY SIGNAL
6V
N-th STAGE PIXEL SIGNAL
(odd)
13V
N-th STAGE PIXEL SIGNAL
10V
FULL-LINE PRECHARGE GRAY SIGNAL
-8V
2V
DOT-SEQUENTIAL PRECHARGE BLACK SIGNAL
5V
DOT-SEQUENTIAL PRECHARGE GRAY SIGNAL
(N+1)-th STAGE PIXEL SIGNAL
(even)

FIG. 8

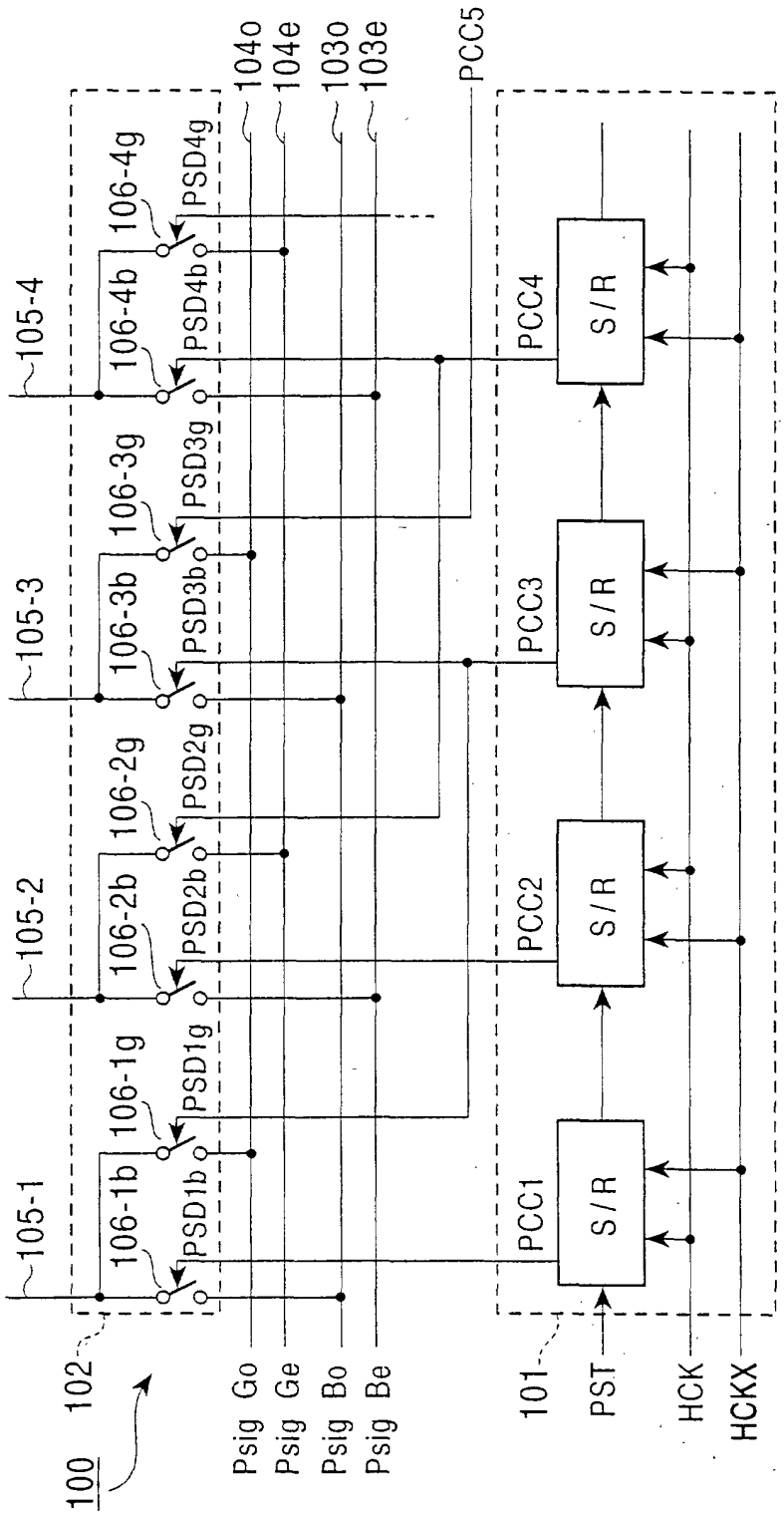

100
102
101
105-1
105-2
105-3
105-4
106-1b
106-1g
106-2b
106-2g
106-3b
106-3g
106-4b
106-4g
PSD1b
PSD1g
PSD2b
PSD2g
PSD3b
PSD3g
PSD4b
PSD4g
1040
104e
1030
103e
PCC5
PCC1
PCC2
PCC3
PCC4
S/R
Psig Go
Psig Ge
Psig Bo
Psig Be
PST
HCK
HCKX

FIG. 9

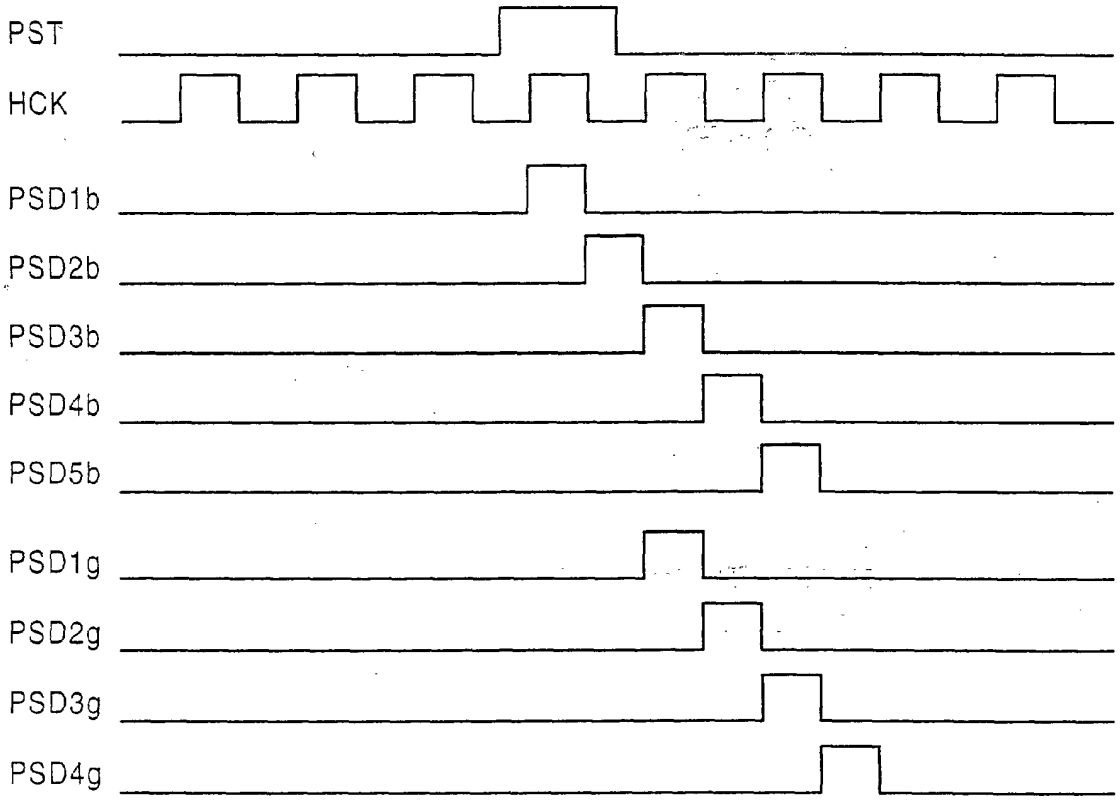

PST
HCK
PSD1b
PSD2b
PSD3b
PSD4b
PSD5b
PSD1g
PSD2g
PSD3g
PSD4g

FIG. 10

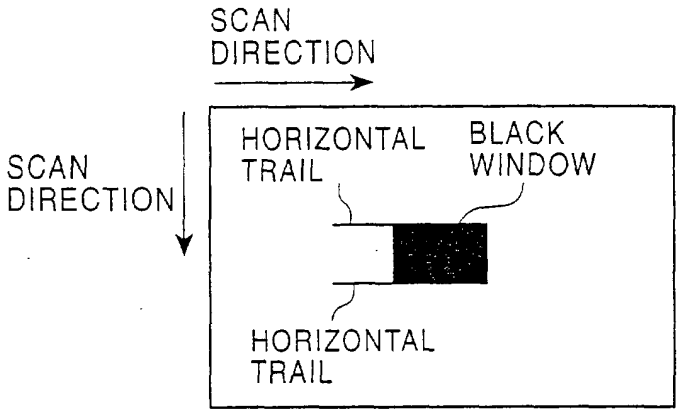

SCAN
DIRECTION
SCAN
DIRECTION
HORIZONTAL
TRAIL
BLACK
WINDOW
HORIZONTAL
TRAIL

FIG. 11

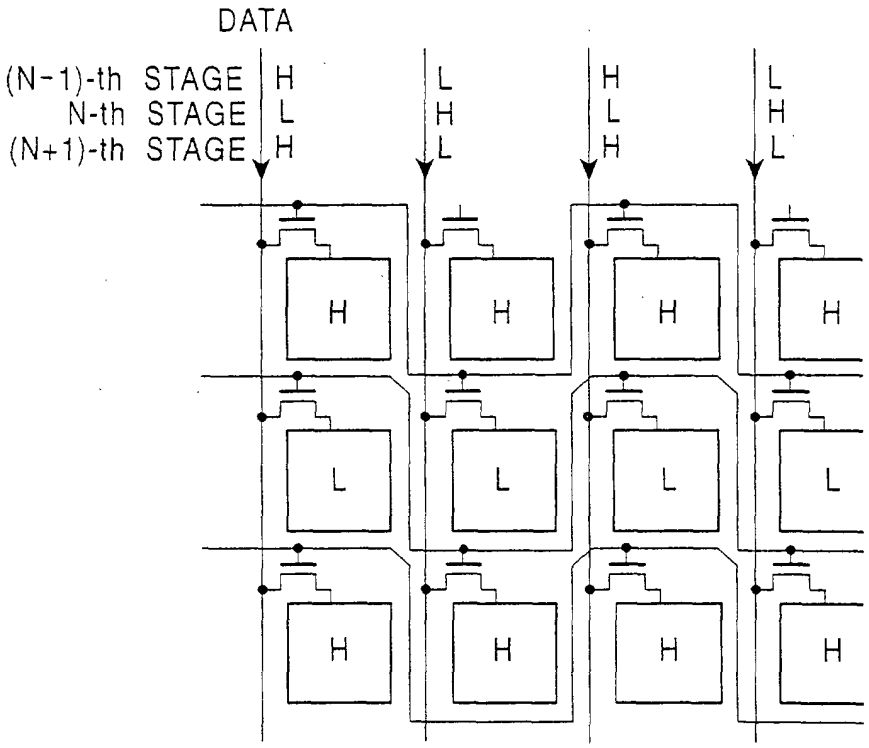

DATA
(N-1)-th STAGE
N-th STAGE
(N+1)-th STAGE
H
L
H
L
H
L
H
L
H
L
H
L
H
H
H
H
L
L
L
L
H
H
H
H

FIG. 12

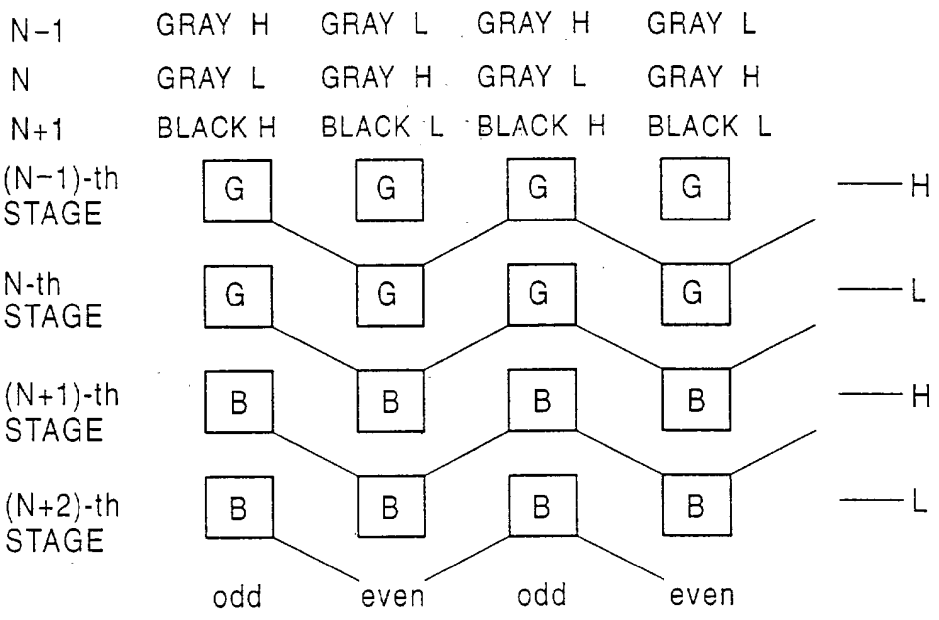
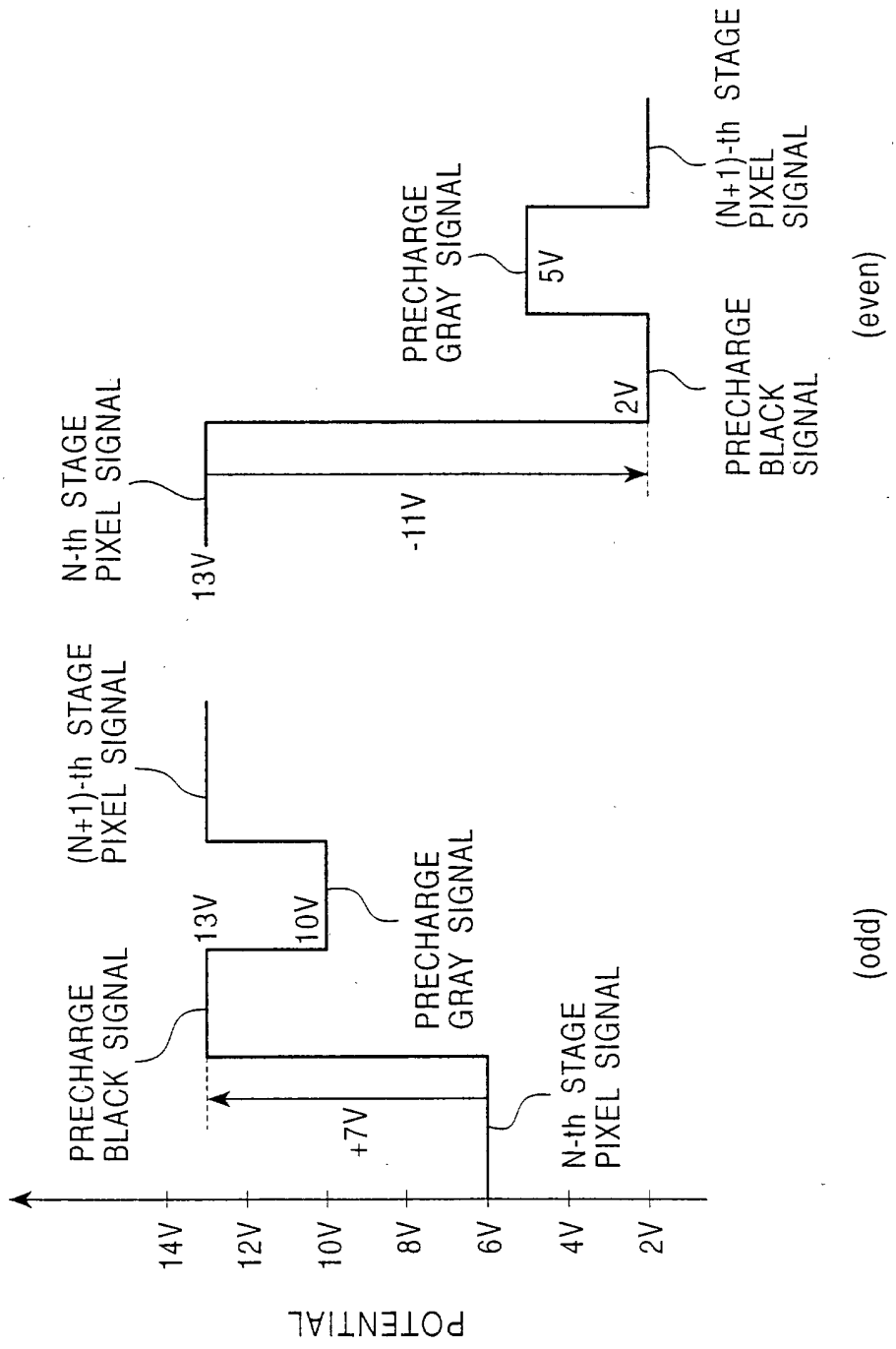

N-1
GRAY H
GRAY L
GRAY H
GRAY L
N
GRAY L
GRAY H
GRAY L
GRAY H
N+1
BLACK H
BLACK L
BLACK H
BLACK L
(N-1)-th STAGE
N-th STAGE
(N+1)-th STAGE
(N+2)-th STAGE
G
B
H
L
odd
even
odd
even

FIG. 13


POTENTIAL
14V
12V
10V
8V
6V
4V
2V
PRECHARGE BLACK SIGNAL
13V
10V
PRECHARGE GRAY SIGNAL
+7V
N-th STAGE PIXEL SIGNAL
(N+1)-th STAGE PIXEL SIGNAL
(odd)
N-th STAGE PIXEL SIGNAL
13V
-11V
PRECHARGE GRAY SIGNAL
5V
2V
PRECHARGE BLACK SIGNAL
(N+1)-th STAGE PIXEL SIGNAL
(even)